Amendments to the Claims:

Please replace all prior versions, and listings of claims in the application with the following listing of claims.

Listing of claims

Claim 1 (currently amended): Apparatus for use in a computer system comprising:

a pipeline bus architecture, in which data traverses the bus architecture over a plurality of system clock cycles;

a plurality of modules connected to the bus architecture;

wherein the bus architecture comprises:

a plurality of bus connection units; and

a plurality of bus portions arranged in series, each bus portion, except the last in the series, being connected to the next portion in the series by way of a bus ~~connecting~~ connection unit,

wherein each of the modules is connected to the bus architecture by way of a respective one of the bus connection units, and

each of the bus connection units including multiplexer circuitry for selectively connecting a module to the bus architecture.

Claim 2 (currently amended): Apparatus as claimed in claim 1, wherein each bus connection unit includes output circuitry connected to the bus portions to which the unit is connected, the output circuitry being ~~optimised~~ tailored to optimize the signal characteristics for the length of the bus portions concerned.

Claim 3 (original): Apparatus as claimed in claim 1, wherein the bus portions are all equal in length.

Claim 4 (currently amended): Apparatus as claimed in claim 1, wherein the pipeline bus architecture comprises a primary pipelined bus and a secondary pipelined bus, the primary and secondary buses being interconnected by an interface, a first plurality [[or]] of modules connected to the primary bus by means of respective said bus connection units, and a second

plurality of modules connected to the secondary bus by means of respective said bus connection units.

Claim 5 (original): Apparatus as claimed in claim 1, wherein a central arbitration unit arbitrates between the modules in order to grant access to the bus architecture.

Claim 6 (original): Apparatus as claimed claim 5, wherein the pipelined bus architecture comprises a primary pipelined bus and a secondary pipelined bus, the primary and secondary buses interconnected by an interface, a first plurality of modules connected to the primary bus by means of respective said bus connection units, and a second plurality of modules connected to the secondary bus by means of respective said bus connection units.

Claim 7 (original): Apparatus as claimed in claim 4, wherein the first plurality of modules are latency intolerant and the second plurality of modules are latency tolerant.

Claim 8 (currently amended): Apparatus as claimed in claim 4, wherein the primary bus [[is]] has a length of one pipeline stage, ~~as herein defined, in length~~ said length being the bus length traveled by a data pulse in a single system clock cycle.

Claim 9 (original): Apparatus as claimed in claim 1, wherein transactions involving data in excess of a predetermined size are split into a plurality of data packets of fixed size, said packets being independently arbitrated.

Claim 10 (currently amended): Apparatus as claimed in [[any]] claim 1 ~~comprising~~ wherein said bus architecture comprises separate read, write and transaction buses.

Claim 11 (original): Apparatus as claimed in claim 1, wherein the bus architecture has a width sufficient to permit read and write request transactions to alternate in successive system clock cycles.

Claim 12 (original): A computer system comprising apparatus as claimed in claim 1.